1. An electrostatic discharge circuit connected between a first power supply voltage source and a second power supply voltage source to protect internal integrated circuits from damage due to an electrostatic discharge, said electrostatic discharge circuit comprising:

a plurality of serially connected polycrystalline silicon diodes formed on a surface of a substrate, each diode having a first electrode and second electrode, said plurality of serially connected polycrystalline diodes including a first diode of the plurality of diodes has its first electrode connected to the first power supply voltage source, and a last diode having its second electrode connected to the second power supply voltage source,

wherein the first electrode is a first region of a polycrystalline silicon being heavily doped with an impurity of a first type and the second electrode is a second region of a polycrystalline silicon being heavily doped with an impurity of a second type, said second region being adjoined to the first region to form an electrical junction.

2. The electrostatic discharge circuit of claim 1 wherein the adjoined first and second regions of each diode are formed on shallow trench isolation formed within the substrate.

3. The electrostatic discharge circuit of claim 1 wherein each diode further comprises a resistor protection oxide formed to overlay a portion of the first and second regions at the junction.

4. The electrostatic discharge circuit of claim 1 wherein the first electrode of each polycrystalline silicon diode is a cathode and the second electrode of each polycrystalline silicon diode is an anode.

5. The electrostatic discharge circuit of claim 4 wherein the impurity of the first type is an N-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

6. The electrostatic discharge circuit of claim 4 wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

7. The electrostatic discharge circuit of claim 4 wherein each of the polycrystalline diodes has a thickness of from approximately 1000Å to approximately 3000 Å.

8. The electrostatic discharge circuit of claim 4 wherein each of the polycrystalline diodes has a thickness of from approximately 0.5μm to approximately 100μm.

9. The electrostatic discharge circuit of claim 1 wherein a number of the plurality of serially connected polycrystalline silicon diodes is determined by the formula:

$$n \geq \frac{V_{noise} + |Vx1 - Vx2|}{V_T}$$

where:

n is the number serially connected of polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuits between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,

Vx2 is the magnitude of the second power supply voltage source, and

V_T is the threshold voltage of each polycrystalline silicon diodes.

10. An integrated circuit formed on a substrate comprising:

a first power distribution network connected to a first power supply voltage source;

a second power distribution network connected to a second power supply voltage source;

a plurality of internal circuits connected between the first and second power distribution networks; and

an electrostatic discharge circuit connected between a first power supply voltage source and a second power supply voltage source to protect said internal circuits from an ESD event, said electrostatic discharge circuit comprising:

a plurality of serially connected polycrystalline silicon diodes formed on a surface of a substrate, each diode having a first electrode and second electrode, said plurality of serially connected polycrystalline diodes including a first diode of the plurality of diodes has its first electrode connected to the first power supply voltage source, and a last diode having its second electrode connected to the second power supply voltage source,

wherein the first electrode is a first region of a polycrystalline silicon being heavily doped with an impurity of a first type and the second electrode is a second region of a polycrystalline silicon being heavily doped with an impurity of a second type, said second region being adjoined to the first region to form an electrical junction.

11. The integrated circuit of claim 10 wherein the adjoined first and second regions of each diode are formed on shallow trench isolation formed within the substrate.

12. The integrated circuit of claim 10 wherein each diode further comprises a resistor protection oxide formed to overlay a portion of the first and second regions at the junction

13. The integrated circuit of claim 10 wherein the first electrode of each polycrystalline silicon diode is a cathode and the second electrode of each polycrystalline silicon diode is an anode.

14. The integrated circuit of claim 13 wherein the impurity of the first type is an N-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

15. The integrated circuit of claim 13 wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

16. The integrated circuit of claim 13 wherein each of the polycrystalline diodes has a thickness of from approximately 1000Å to approximately 3000 Å.

17. The integrated circuit of claim 13 wherein each of the polycrystalline diodes has a thickness of from approximately 0.5μm to approximately 100μm.

18. The integrated circuit of claim 10 wherein a number of the plurality of serially connected polycrystalline silicon diodes is determined by the formula:

$$n \geq \frac{V_{noise} + |Vx1 - Vx2|}{V_T}$$

where:

n is the number of serially connected polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuits between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,

Vx2 is the magnitude of the second power supply voltage source, and

V_T is the threshold voltage of each polycrystalline silicon diodes.

19. A method for forming an electrostatic discharge circuit comprising serially connected polycrystalline silicon diodes, said method comprising the steps of:

providing a substrate;

forming polycrystalline silicon members upon said substrate:

doping a first portion of each of said polycrystalline silicon members with an impurity of a first type;

doping a second portion of each of said polycrystalline silicon members with an impurity of a second type such that a junction is formed where the first portion of each of said polycrystalline silicon members adjoins said second portion of said polycrystalline members;

connecting the second portion of one polycrystalline section to the first portion of a subsequent polycrystalline silicon member;

connecting the first portion of a first polycrystalline silicon member to a first power supply voltage source; and

connecting the second portion of a last polycrystalline silicon member to a second power supply voltage source.

20. The method of claim 19 further comprising the step of:

forming a plurality of shallow trench isolation regions, each polycrystalline silicon member being formed on one of said isolation regions.

21. The method of claim 19 further comprising the step of:

forming a resistor protection oxide member upon each of the polycrystalline silicon members to overlay said junction.

22. The method of claim 19 wherein the connecting the first and second portions of the polycrystalline silicon members comprises the steps of:

alloying a metal into top surfaces of the first and second portions of each of the polycrystalline silicon members to form contact areas; and

forming connecting metallization in contact with the contact areas of the first and second portions of each polycrystalline silicon member and between the second portion of each polycrystalline

silicon member and the first portion of the subsequent polycrystalline silicon member, the first portion of the first polycrystalline silicon member, and the second portion of the last polycrystalline silicon member.

23. The method of claim 19 wherein the first portion of each of the polycrystalline silicon members is a cathode of each polycrystalline silicon diode and the second portion of each of the polycrystalline members is an anode of each polycrystalline silicon diode.

24. The method of claim 19 wherein the impurity of the first type is an N-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

25. The method of claim 19 wherein the impurity of the second type is a P-type impurity having a density of from approximately 10^{15} atoms/cm^{-3} to approximately 10^{21} atoms/cm^{-3}.

26. The method of claim 19 wherein each of the polycrystalline silicon members has a thickness of from approximately 1000Å to approximately 3000 Å.

27. The method of claim 19 wherein each of the polycrystalline silicon members has a thickness of from approximately 0.5μm to approximately 100μm.

28. The method of claim 19 wherein a number of the serially connected polycrystalline silicon diodes is determined by the formula:

$$n \geq \frac{V_{noise} + |Vx1 - Vx2|}{V_T}$$

where:

n is the number serially connected of polycrystalline silicon diodes,

V_{noise} is the maximum voltage level difference allowed to be present on the internal integrated circuits between the first power supply voltage source and the second power supply voltage source,

Vx1 is the magnitude of the first power supply voltage source,

Vx2 is the magnitude of the second power supply voltage source, and

V_T is the threshold voltage of each polycrystalline silicon diodes.